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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,595	11/19/2003	Masayoshi Kusumoto	1448.1046	6448

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EXAMINER	
SAVLA, ARPAN P	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 01/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,595	KUSUMOTO ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/19/03, 12/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/715595 has a total of 27 claims pending in the application, there are 2 independent claims and 25 dependent claims, all of which are ready for examination by Examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

2. As required by MPEP § 201.14(c), acknowledgment is made of Applicant's claim for priority based on an application filed in the Japanese Patent Office on December 26, 2002.

INFORMATION CONCERNING DRAWINGS

Drawings

3. Applicant's drawings submitted November 19, 2003 are acceptable for examination purposes.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

4. As required by MPEP § 609(c), Applicant's submission of the Information Disclosure Statements dated November 19, 2003 and December 15, 2003 are acknowledged by Examiner and cited references have been considered in the examination of the claims now pending. As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

OBJECTIONS

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: "A Microcomputer Which Converts Interrupt Vector Addresses To Alternate Interrupt Vector Addresses During The Rewriting Of A Program."

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. **Claims 2-3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.** Claims 2-3 recite the limitation "the

interrupt vector address" on page 15, lines 22-23 and page 16, line 6. There is insufficient antecedent basis for this limitation in the claims. Applicant may consider amending the claim to read "the address indicating a storage place of the interrupt vector."

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 4, 6-12, 15-17, 19-25 are rejected under 35 U.S.C. 103(a) as being obvious over Yamada et al. (U.S. Patent 5,950,222) in view of Iwata (U.S. Patent 5,881,295).

10. **As per claim 1**, Yamada discloses a microcomputer comprising:

a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently (col. 3, lines 12-19; Fig. 1, element 1); It should be noted that "EEPROM" is analogous to "nonvolatile memory", "region A" is analogous to "first storage area", and "region B" is analogous to "second storage area."

wherein a plurality of interrupt vectors indicating respective storage places of a plurality of interrupt programs executed upon requesting of an interrupt is stored in the first storage area (col. 8, lines 25-29; Fig. 8, elements (31-1)~(31-n));

and a plurality of alternate interrupt vectors corresponding to the respective interrupt vectors is stored in the second storage area (col. 8, lines 22-25; Fig. 8, elements (30-1)~(30-n));

a central processing unit that has a mechanism to access the nonvolatile memory (col. 3, lines 19-23 and 28-29; Fig. 1, element 2).

Yamada does not expressly disclose a flag indicating that the first storage area is not accessible;

and a conversion circuit that, based on a state of the flag, converts an address indicating a storage place of the interrupt vector that is accessed by the central processing unit into an address indicating a storage place of the corresponding alternate interrupt vector.

Iwata discloses a flag indicating that the first storage area is not accessible (col. 9, lines 51-55 and 58-61; col. 10, lines 50-58; Fig. 1, element 18); It should be noted that when the built-in ROM is in boot or user program mode the contents of the built-in ROM are not accessible. MS0 and MS1 are flags indicating whether the built-in ROM is in boot or user program mode respectively, therefore, MS0 and MS1 are also flags that indicate the built-in ROM is not accessible.

and a conversion circuit that, based on a state of the flag, converts an address indicating a storage place of the interrupt vector that is accessed by the central

processing unit into an address indicating a storage place of the corresponding alternate interrupt vector (col. 14, lines 6-15; Fig. 5).

Yamada and Iwata are analogous because they are from the same field of endeavor, that being microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Iwata's conversion circuit within Yamada's microcomputer.

The motivation for doing so would have been to improve the safety of a system during on-board programming of a program memory (Iwata, col. 3, lines 25-27). Also, another motivation for doing so would have been to provide additional safety by preventing a microcomputer from running away and from being damaged even when an interrupt handling or exception handling is requested during on-board programming of the above program memory (Iwata, col. 3, lines 31-34).

Therefore, it would have been obvious to combine Yamada and Iwata for the benefit of obtaining the invention as specified in claim 1.

11. **As per claim 4**, Iwata discloses the conversion circuit comprises hardware that performs a predetermined conversion operation (col. 14, lines 19-35; Fig. 5).

12. **As per claim 6**, Iwata discloses the nonvolatile memory, the central processing unit, the flag, and the interrupt vector address conversion circuit are integrated on a same semiconductor chip (col. 6, lines 46-50; Fig. 1, element 30).

13. **As per claim 7**, Yamada discloses the interrupt program is stored in the first storage area, the interrupt vector stores a start address of the interrupt program, the alternate interrupt program that is executed instead of the interrupt program is stored in

the second storage area, and the alternate interrupt vector stores a start address of the alternate interrupt program (col. 8, lines 14-29; Fig. 1, element 1). It should be noted that it is inherently required an interrupt vector store the starting address of it's corresponding interrupt handler routine (interrupt program).

14. **As per claim 8**, Iwata discloses the interrupt program is stored in the second storage area, and the interrupt vector and the alternate interrupt vector store a start address of the interrupt program (col. 17, lines 50-58; col. 17, line 66 – col. 18, line 3; Fig. 1, element 13). It should be noted that "built-in RAM" is analogous to "second storage area", "NMI handling routine RB" is analogous to "interrupt program", "vector address NMIA" is analogous to "interrupt vector", and "vector address NMIB" is analogous to "alternate interrupt vector." It should also be noted that when in user program mode or boot mode both NMIA and NMIB, which are stored in the built-in RAM, access NMI handling routine RB.

15. **As per claim 9**, Yamada discloses the microcomputer according to claim 7.

Yamada does not expressly disclose a main program is stored in the first storage area.

Iwata discloses a main program is stored in the first storage area (col. 9, lines 8-9; Fig. 1, element 18). It should be noted that "built-in ROM" is analogous to "first storage area."

16. **As per claim 10**, Iwata discloses a main program is stored in the first storage area (col. 9, lines 8-9; Fig. 1, element 18).

17. **As per claim 11**, Yamada discloses the microcomputer according to claim 7.

Yamada does not expressly disclose a main program is stored in the second storage area.

Iwata discloses a main program is stored in the second storage area (col. 10, lines 15-17; Fig. 1, element 13).

18. **As per claim 12**, Iwata discloses a main program is stored in the second storage area (col. 10, lines 15-17; Fig. 1, element 13).

19. **As per claim 15**, Yamada discloses a microcomputer comprising:

a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently (col. 3, lines 12-19; Fig. 1, element 1); See citation note for claim 1.

wherein a plurality of interrupt vectors indicating respective storage places of a plurality of interrupt programs executed upon requesting of an interrupt is stored in the first storage area (col. 8, lines 25-29; Fig. 8, elements (31-1)~(31-n));

and a plurality of alternate interrupt vectors corresponding to the respective interrupt vectors is stored in the second storage area (col. 8, lines 22-25; Fig. 8, elements (30-1)~(30-n));

a central processing unit that has a mechanism to access the nonvolatile memory (col. 3, lines 19-23 and 28-29; Fig. 1, element 2).

Yamada does not expressly disclose a flag indicating that the first storage area is not accessible;

and a conversion circuit that, based on a state of the flag, performs address conversion so that an area including the interrupt vector accessed by the central

processing unit in the first storage area is replaced with an area including the corresponding alternate interrupt vector in the second storage area.

Iwata discloses a flag indicating that the first storage area is not accessible (col. 9, lines 51-55 and 58-61; col. 10, lines 50-58; Fig. 1, element 18); See citation note for claim 1.

and a conversion circuit that, based on a state of the flag, performs address conversion so that an area including the interrupt vector accessed by the central processing unit in the first storage area is replaced with an area including the corresponding alternate interrupt vector in the second storage area (col. 10, lines 61-64; Fig. 1, elements 13 and 18). It should be noted that "moved to" is analogous to "replaced."

20. **As per claim 16**, Iwata discloses the conversion circuit performs address conversion individually for a plurality of areas including each of the interrupt vectors (col. 11, lines 34-38).

21. **As per claim 17**, Iwata discloses the conversion circuit comprises hardware that performs a predetermined conversion operation (col. 11, line 65 – col. 12, line 21; Fig. 3).

22. **As per claim 19**, Iwata discloses the nonvolatile memory, the central processing unit, the flag, and the interrupt vector address conversion circuit are integrated on a same semiconductor chip (col. 6, lines 46-50; Fig. 1, element 30).

23. **As per claim 20**, Yamada discloses the interrupt program is stored in the first storage area, the interrupt vector stores a start address of the interrupt program, the

alternate interrupt program that is executed instead of the interrupt program is stored in the second storage area, and the alternate interrupt vector stores a start address of the alternate interrupt program (col. 8, lines 14-29; Fig. 1, element 1). See citation note for claim 7.

24. **As per claim 21**, Iwata discloses the interrupt program is stored in the second storage area, and the interrupt vector and the alternate interrupt vector store a start address of the interrupt program (col. 17, lines 50-58; col. 17, line 66 – col. 18, line 3; Fig. 1, element 13). See citation note for claim 8.

25. **As per claim 22**, Yamada discloses the microcomputer according to claim 20.

Yamada does not expressly disclose a main program is stored in the first storage area.

Iwata discloses a main program is stored in the first storage area (col. 9, lines 8-9; Fig. 1, element 18). See citation note for claim 9.

26. **As per claim 23**, Iwata discloses a main program is stored in the first storage area (col. 9, lines 8-9; Fig. 1, element 18).

27. **As per claim 24**, Yamada discloses the microcomputer according to claim 20.

Yamada does not expressly disclose a main program is stored in the second storage area.

Iwata discloses a main program is stored in the second storage area (col. 10, lines 15-17; Fig. 1, element 13).

28. **As per claim 25**, Iwata discloses a main program is stored in the second storage area (col. 10, lines 15-17; Fig. 1, element 13).

29. Claims 5 and 18 are rejected under 35 U.S.C. 103(a) as being obvious over Yamada in view of Iwata as applied to claims 1 and 15 above, and further in view of Andrew S. Tanenbaum, Structured Computer Organization, 2nd Edition, hereafter "Tanenbaum."

30. **As per claims 5 and 18**, Yamada/Iwata discloses the conversion circuit performs a predetermined conversion operation based on a setting by a hardware (Iwata, col. 14, lines 36-54; Fig. 5). It should be noted that the conversion is performed based on the settings of the logic circuits and selection circuits (i.e. hardware).

Yamada/Iwata does not expressly disclose the conversion circuit performs a predetermined conversion operation based on a setting by a software.

Tanenbaum discloses that hardware and software are logically equivalent (pg. 11, line 11).

Yamada/Iwata and Tanenbaum are analogous art because they are from the same field of endeavor, that being computer systems design.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to follow Tanenbaum's argument and base Yamada/Iwata's conversion operation on software settings.

The motivation for doing so would have been to optimize such factors as cost, speed, and reliability (Tanenbaum, pg. 11, lines 14-15).

Therefore, it would have been obvious to combine Yamada/Iwata and Tanenbaum for the benefit of obtaining the invention as specified in claims 5 and 18.

31. Claims 13-14 and 26-27 are rejected under 35 U.S.C. 103(a) as being obvious over Yamada in view of Iwata as applied to claims 7-8 and 20-21, and further in view of Fudeyasu et al. (U.S. Patent 6,154,837).

32. As per claims 13-14 and 26-27, Yamada/Iwata disclose all the limitations of claims 13-14 and 26-27 except a main program is stored in a memory other than the nonvolatile memory.

Fudeyasu discloses a main program is stored in a memory other than the nonvolatile memory (col. 3, lines 37-41; col. 4, lines 25-28; Fig. 1, elements 2 and 4). It should be noted that "boot ROM" is analogous to "nonvolatile memory."

Yamada/Iwata and Fudeyasu are analogous art because they are from the same field of endeavor, that being interrupt processing within microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Fudeyasu's RAM within Yamada/Iwata's microcomputer.

The motivation for doing so would have been to offer the advantage of being able to provide a microcomputer that can achieve effective interrupt processing in boot mode by enabling an erase/write program to execute interrupt processing freely (Fudeyasu, col. 5, lines 5-9).

Therefore, it would have been obvious to combine Yamada/Iwata and Fudeyasu for the benefit of obtaining the inventions as specified in claims 13-14 and 26-27.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

The following references disclose **microcomputers**.

U.S. Patent Number

5,592,652

6,128,751

6,223,265

6,453,397

6,587,916

U.S. Patent Application Publication Number

2002/0144052

2002/0144053

Non-Patent Literature

Fang, W.C., "A System-on-a-Chip Design of a Low-Power Smart Vision System", Oct. 8-10, 1998, IEEE Workshop on Signal Processing Systems, pp. 63-72.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-27** have received a first action on the merits and are subject of a first action non-final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Assistant Examiner
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January 11, 2006

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